## LISTING OF THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Original) A connector chip comprising a rectangular parallelepiped insulating substrate having six surfaces, and a conductive path continuously formed on four continuous surfaces of the six surfaces, no conductive path being formed on remaining two opposing surfaces of the six surfaces.

2. (Original) The connector chip according to claim 1, wherein the conductive path is constituted by forming one or more plated layers over a base layer made of a metal thick film or a metal thin film.

3. (Original) A circuit device comprising a first circuit substrate having a plurality of electrodes formed on a front surface thereof,

a second circuit substrate arranged above the first circuit substrate with a gap provided therebetween and having a plurality of electrodes formed on a rear surface thereof, and

a plurality of connector chips having conductive paths formed thereon,

the electrodes on the first circuit substrate and the electrodes on the second circuit substrate being electrically connected respectively by the connector chips,

the conductive paths and the electrodes being connected by soldering,

the gap being maintained by the connector chips,

each of the connector chips comprising a rectangular parallelepiped insulating substrate having six surfaces, and the conductive path, the conductive path being continuously formed on four continuous surfaces of the six surfaces, no conductive path being formed on remaining two opposing surfaces of the six surfaces.

4. (Original) A connector chip comprising a rectangular parallelepiped insulating substrate having six surfaces, and a plurality of conductive paths formed on an outer peripheral surface, which is constituted by four continuous surfaces of the six surfaces, at a predetermined interval in an opposing direction of reaming two opposing surfaces of the six surface, and running round on the outer peripheral surface.

5. (Original) The connector chip according to claim 4, wherein each of the conductive paths is constituted by forming one or more plated layers over a base layer made of a metal thick film or a metal thin film.

6. (Original) The connector chip according to claim 4, wherein on at least a pair of the surfaces opposing to each other among the four surfaces, insulating layers having a property of repelling molten solder are formed respectively between portions of two adjoining conductive paths among the plurality conductive paths, located on the pair of the surfaces.

7. (Original) The connector chip according to claim 6, wherein the insulating layers formed on one surface of the pair of the surfaces and the insulating layers formed on the other surface of the pair of the surfaces have different colors.

8. (Original) The connector chip according to claim 4, wherein in the insulating substrate, a plurality of conductive-path-formed portions where the conductive paths are formed and a plurality of conductive-path-unformed portions where the conductive paths are not formed are alternately arranged along a center line so that the conductive-path-formed portions and the conductive-path-unformed portions share the center line; and

a width of each of the conductive-path-formed portions orthogonal to the center line is smaller than a width of each of the conductive-path-unformed portions orthogonal to the center line.

9. (Original) The connector chip according to claim 4, wherein in the insulating substrate, a plurality of conductive-path-formed portions where the conductive paths are formed and a plurality of conductive-path-unformed portions where the conductive paths are not formed are alternately arranged along a center line so that the conductive-path-formed portions and the conductive-path-unformed portions share the center line; and

a width of each of the conductive-path-formed portions orthogonal to the center line is larger than a width of each of the conductive-path-unformed portions orthogonal to the center line.

10. (Original) The connector chip according to claim 5, wherein the base layer is formed of a metal thick film including Ag (silver) or a metal thin film of a Ni--Cr (nickel-chromium) alloy or Cu (copper); and

each of the one or more plated layers comprises a first plated layer made of Cu (copper) or Ni (nickel) and a second plated layer made of a Sn (tin) alloy or Sn (tin), formed over the first plated layer.

11. (Withdrawn) A method of manufacturing a connector chip comprising:

preparing a plate-like insulating substrate material with a plurality of through hole rows arranged therein, each of the through hole rows including through holes arranged at a constant interval;

forming a plurality of first base layers on one of both surfaces of the insulating substrate material, and a plurality of second base layers on the other of the both surfaces of the insulating substrate material, each of the first and second base layers being formed between each two of the through holes respectively located in each two adjoining through hole rows, the first base layers and the second base layers being formed of a metal thick film or a metal thin film;

forming insulating layers between each two adjoining first base layers and between each two adjoining second base layers, respectively, the insulating layers having a property of repelling molten solder;

forming third base layers over edge portions of the first base layers located on one side, internal surfaces of the through holes, and edge portions of the second base layers located on the one side, respectively, by metal vapor deposition;

forming fourth base layers over edge portions of the first base layers located

on the other side, the internal surfaces of the through holes, and edge portions of the second base layers located on the other side, respectively, by metal vapor deposition;

cutting the insulating substrate material along substantially a middle of each of the through hole rows; and

forming one or more plated layers over the first to fourth base layers.

12. (Withdrawn) The method of manufacturing a connector chip according to claim 11, wherein the insulating layers formed on one side of the insulating substrate material and the insulating layers formed on the other side of the insulating substrate material are made in different colors; and

breaking slits are formed along substantially the middle of the each of the through hole rows in one side of the insulating substrate material, and the insulating substrate material is cut along the breaking slits.